

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	11628	(PLL or (phase adj lock\$3 adj loop)) same (divid\$3 or counter) same ((phase or frequency) near5 (detector or comparator or discriminator))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/16 14:51
L2	452721	(frame or protocol or SDH or (synchron\$5 near3 hierarchy)) with (identificat\$3 or detect\$3 or control\$4 or monitor\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/16 14:54
L3	1388	1 and 2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/16 14:55
L4	29034	(memory or (shift adj register)) same control\$4 same (oscillator or divider or ((phase or frequency) adj (comparator or detector)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/16 14:57
L5	284	3 and 4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/16 14:58

Day : Friday
Date: 9/16/2005

Time: 16:01:44

 **PALM INTRANET****Inventor Name Search Result**

Your Search was:

Last Name = DAUTH

First Name = FRITZ-JOERG

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09936670	Not Issued	30	01/02/2002	Method and apparatus for automatically producing clock signals for sampling data signals at different data rates via a phase locked loop	DAUTH, FRITZ- JOERG

Inventor Search Completed: No Records to Display.

Search Another: Inventor

Last Name	First Name	
<input type="text" value="DAUTH"/>	<input type="text" value="FRITZ-JOERG"/>	<input type="button" value="Search"/>

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